What is claimed is:

(Claim 1) 1. A circuit layout structure for a chip with a bonding pad area, an adjacent device area, and a substrate comprising:

a plurality of circuit layers, sequentially stacking over the substrate;
a plurality of dielectric layers, each sandwiching between a pair of neighboring circuit layers; and
a plurality of vias, passing through the dielectric layers and electrically connecting various circuit layers,
wherein the circuit layer farthest from the substrate has a plurality of bonding pads within the bonding pad area, and the bonding pads close to the device area overstride at least a non-signal circuit layer within the device area via the circuit layer farthest from the substrate, and then electrically connects with the circuit layer closer to the substrate through the via.

(Claim 2) 2. The circuit layout structure of claim 1, wherein the bonding pads close to the device area comprises a plurality of signal bonding pads.

(Claim 3) 3. The circuit layout structure of claim 1, wherein the bonding pad farther away from the device area comprises a plurality of non-signal bonding pads.

(Claim 4) 4. The circuit layout structure of claim 3, wherein the bonding pads farther from the device area comprises a ground bonding pad.

(Claim 5) 5. The circuit layout structure of claim 3, wherein the bonding pads next to the farthest bonding pads from the device area comprises a power bonding pad.

(Claim 6) 6. The circuit layout structure of claim 1, wherein the circuit layers comprises N circuit layers which N is a natural integer greater than 2,

and the first circuit layer of N circuit layers is set on the substrate, a $(N-1)^{th}$ circuit layer is set on a $(N-2)^{th}$ circuit layer, and a N^{th} circuit layer is set on the $(N-1)^{th}$ circuit layer and the part of the N^{th} circuit layer within the device area forms a direct electrical connection with the bonding pad closest to the device area.

(Claim 7) 7. The circuit layout structure of claim 6, wherein the bonding pad farthest from the device area comprises a ground bonding pad such that the ground bonding pad forms a direct electrical connection with the $(N-2)^{th}$ circuit layer.

(Claim 8) 8. The circuit layout structure of claim 6, wherein the bonding pad next to the farthest bonding pad from the device area comprises a power bonding pad such that the power bonding pad forms a direct electrical connection with the $(N-1)^{th}$ circuit layer.

(Claim 9) 9. The circuit layout structure of claim 6, wherein the bonding pad next to the closest bonding pad to the device area is electrically connected through the $(N-1)^{th}$ circuit layer to the N^{th} circuit layer within the device area.